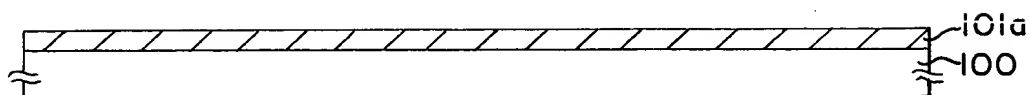


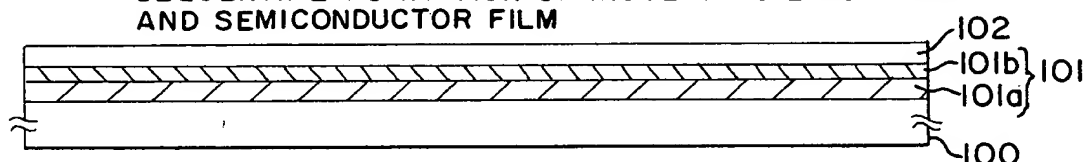
# FIG. 1(A)

FORMATION OF INSULATING LAYER 101a



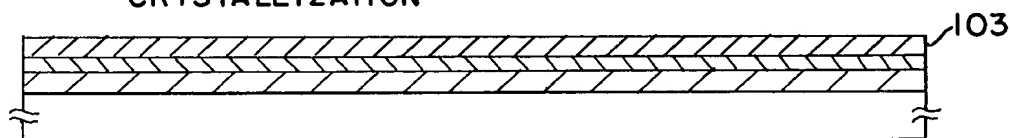
# FIG. 1(B)

SEQUENTIAL FORMATION OF INSULATING LAYER 101b AND SEMICONDUCTOR FILM



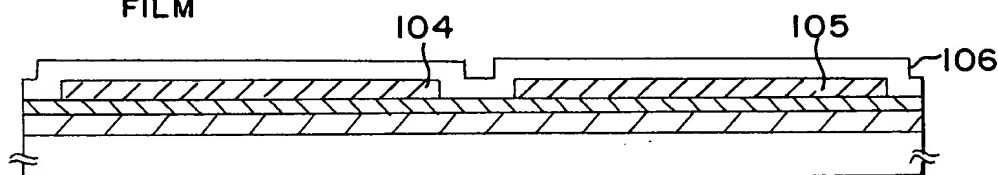
# FIG. 1(C)

CRYSTALLIZATION



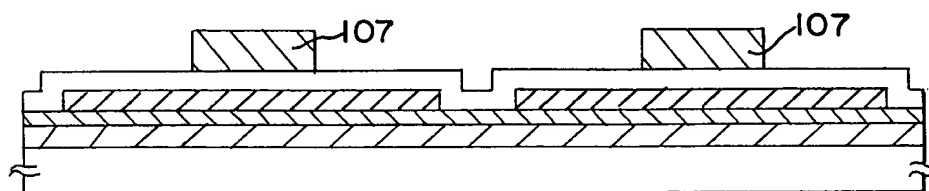
# FIG. 1(D)

FORMATION OF ACTIVE LAYER AND GATE INSULATING FILM

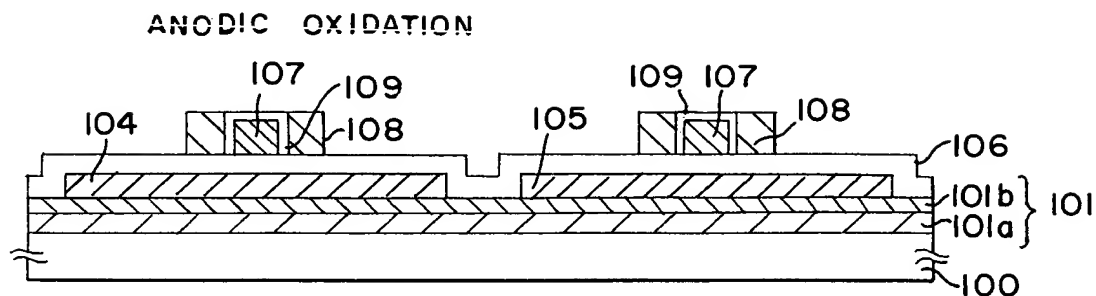


# FIG. 1(E)

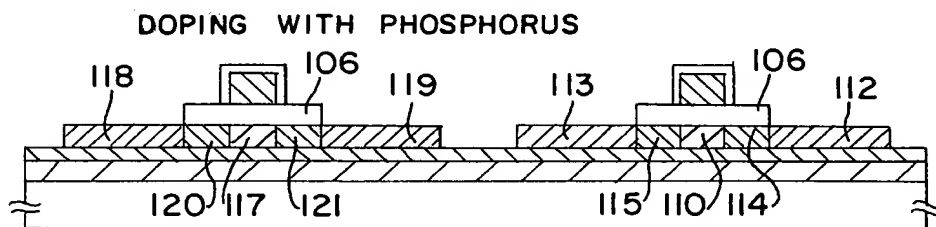
FORMATION OF GATE WIRING



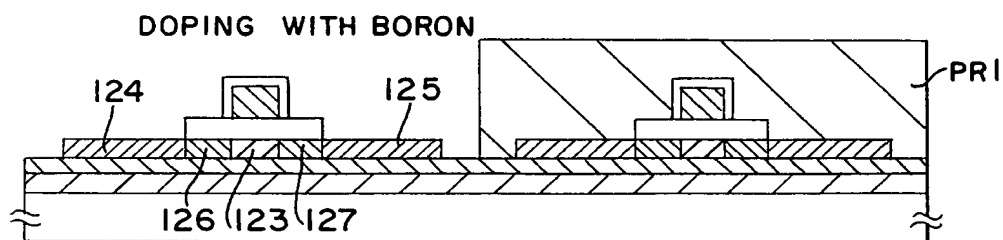
# FIG.2(A)



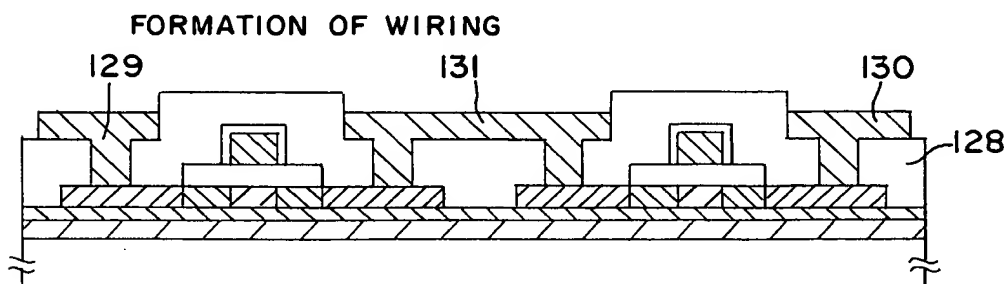
# FIG.2(B)



# FIG.2(C)



# FIG.2(D)



P-CHANNEL TYPE

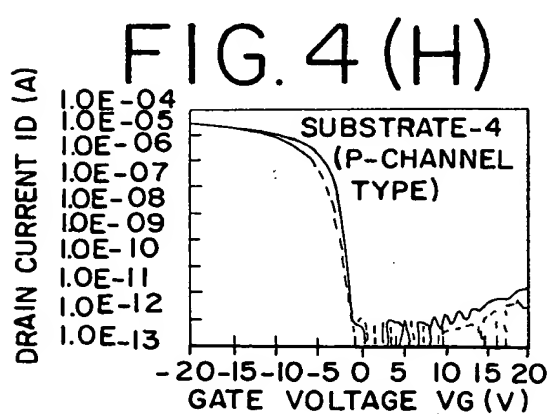
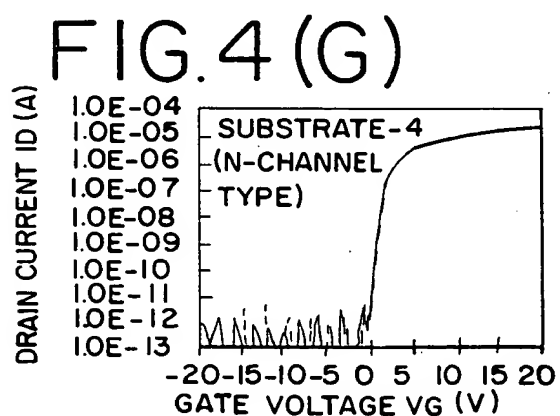
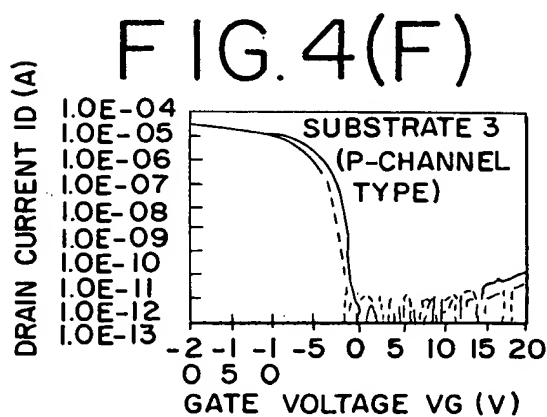
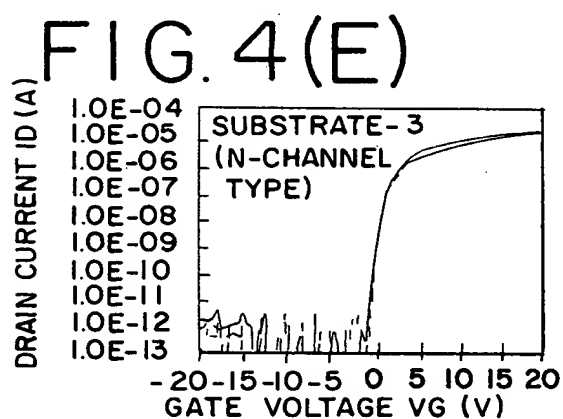
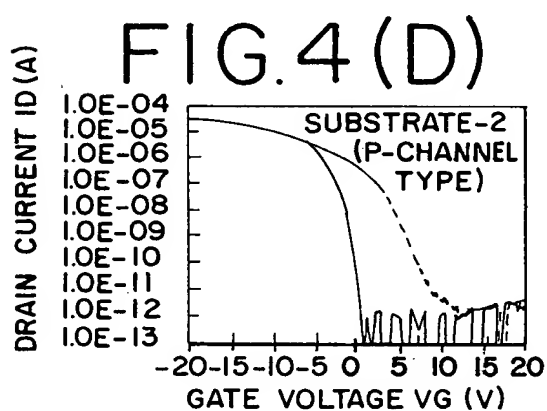
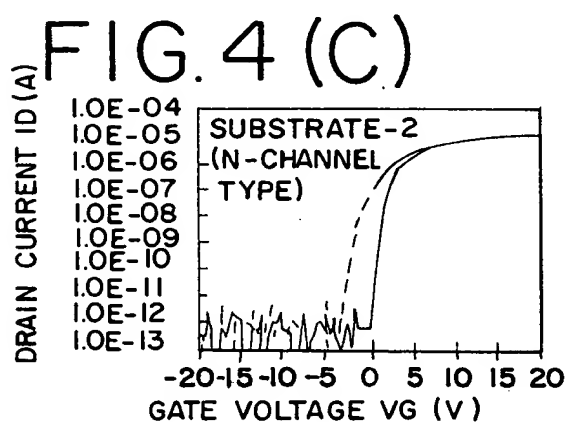
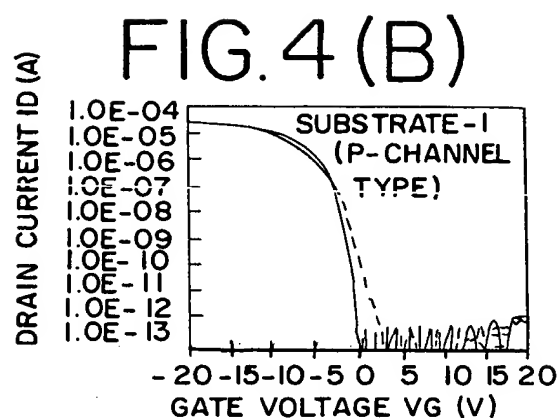
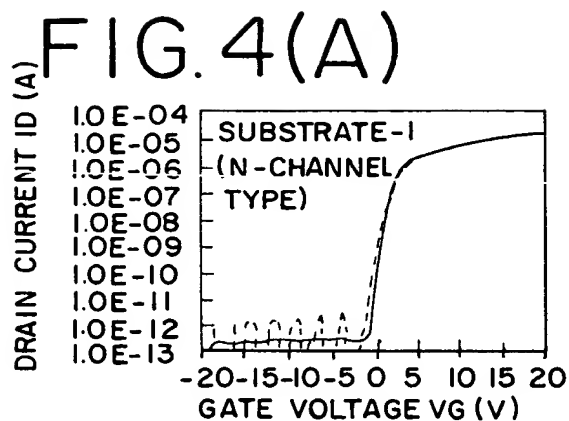
N-CHANNEL TYPE



FIG. 3

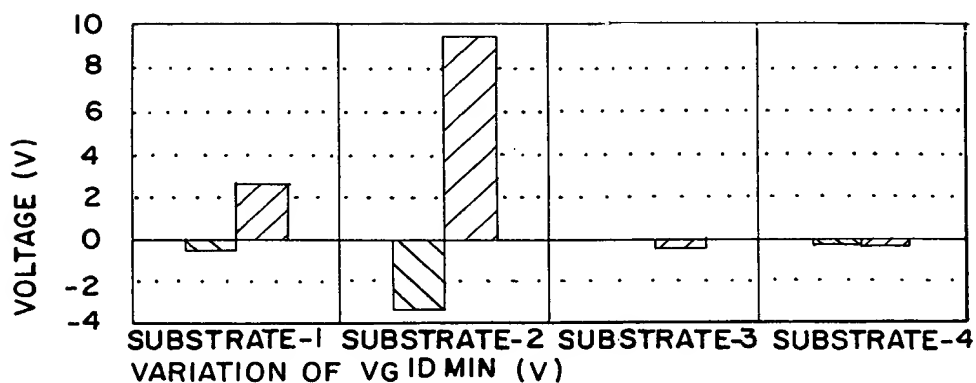
FLOW RATE OF RAW MATERIAL GAS	SUBSTRATE <sub>1</sub>		SUBSTRATE <sub>2</sub>		SUBSTRATE <sub>3</sub>		SUBSTRATE <sub>4</sub>	
	Si H 4		4		10		15	
	N 2 O		400		20		20	
	N H 3		0		100		200	
HEAT TREATMENT			CONDUCTED NO		NO		NO	
COMPOSITION RATIO (ATOMIC %)	N		7.0		24.0		44.1	
	O		59.5		26.5		6.0	
	Si		32.0		33.0		34.4	
	H		1.5		16.5		15.5	
REFRACTIVE INDEX			1.4566		1.7468		1.7975	

FILM FORMING CONDITIONS AND PHYSICAL PROPERTIES  
OF INSULATING LAYER (SILICON OXIDE NITRIDE LAYER) 101a

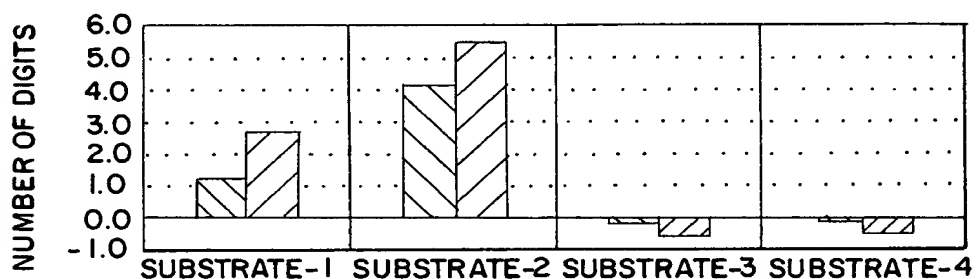


# FIG. 5A

▨ N-CHANNEL TYPE (L/W=5.6/7.5 $\mu$ m)  
▩ P-CHANNEL TYPE (L/W=5.6/7.5 $\mu$ m)



# FIG. 5B



# FIG. 5C

CHANGE OF NUMBER OF DIGITS OF 1 CUT

※ STRESS CONDITIONS

150°C, 1 HOUR,  $V_G$ : 20V (N-CHANNEL TYPE), -20V (P-CHANNEL TYPE),  
 $V_D = V_S = 0V$

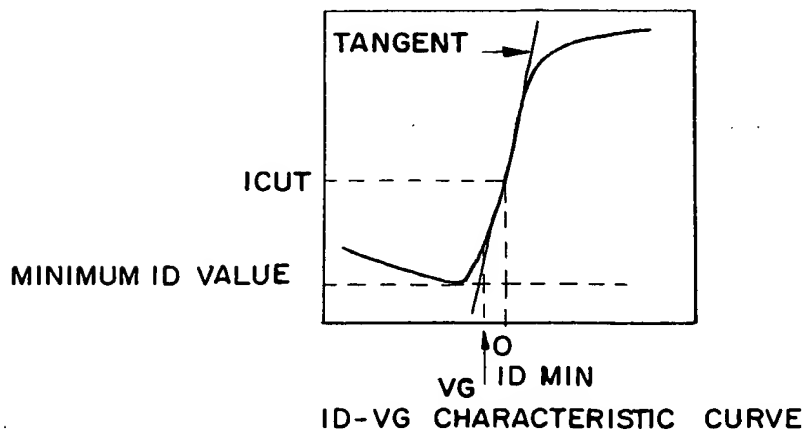


FIG.6

DRIVER CIRCUIT (CMOS CIRCUIT)

PIXEL MATRIX CIRCUIT

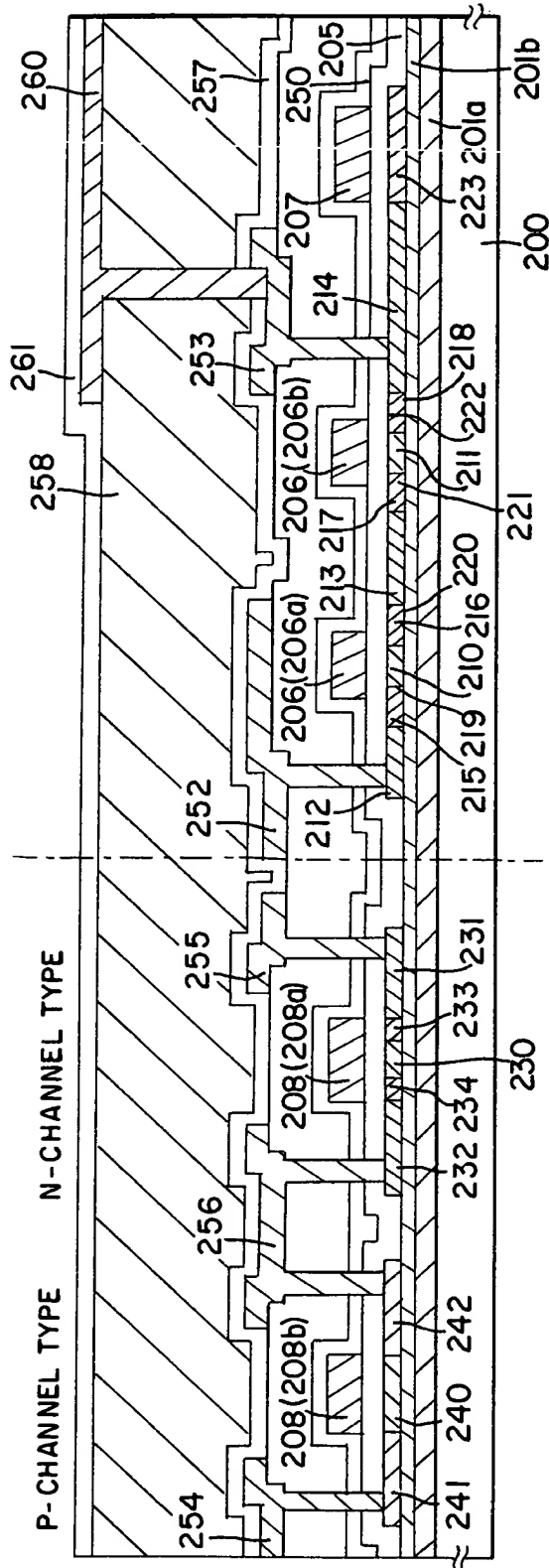


FIG. 7(A)

FORMATION OF UNDERLYING FILM, ACTIVE LAYER AND GATE INSULATING FILM

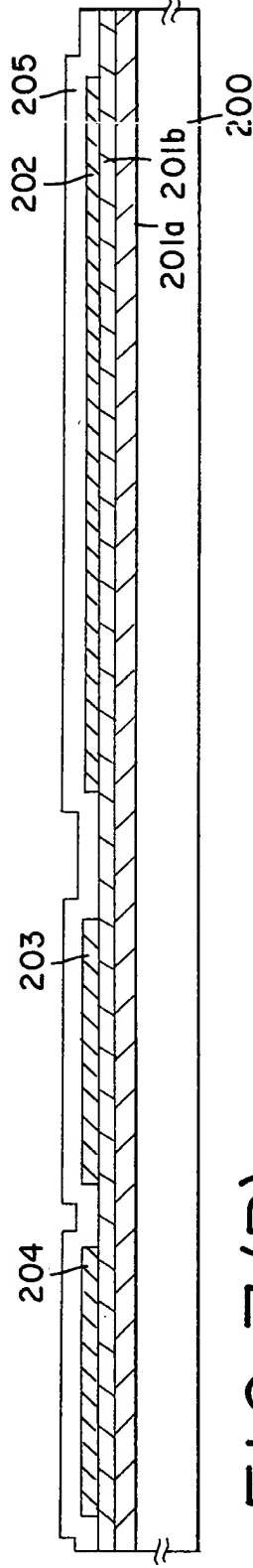


FIG. 7(B)

DOPING PROCESS OF PHOSPHORUS (FORMATION OF n<sup>+</sup>-TYPE REGION)

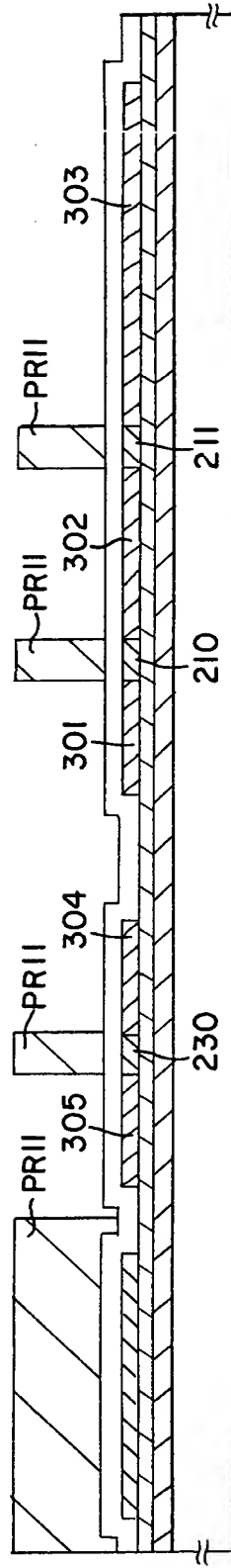


FIG. 7(C)

FORMATION OF CONDUCTIVE FILM

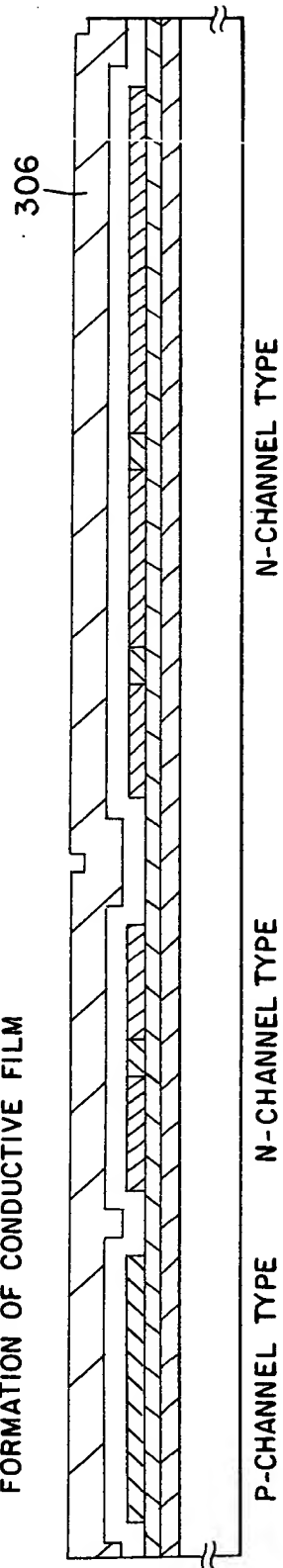


FIG.8(A)

DOPING WITH BORON (FORMATION OF P<sup>+</sup>-TYPE REGION)

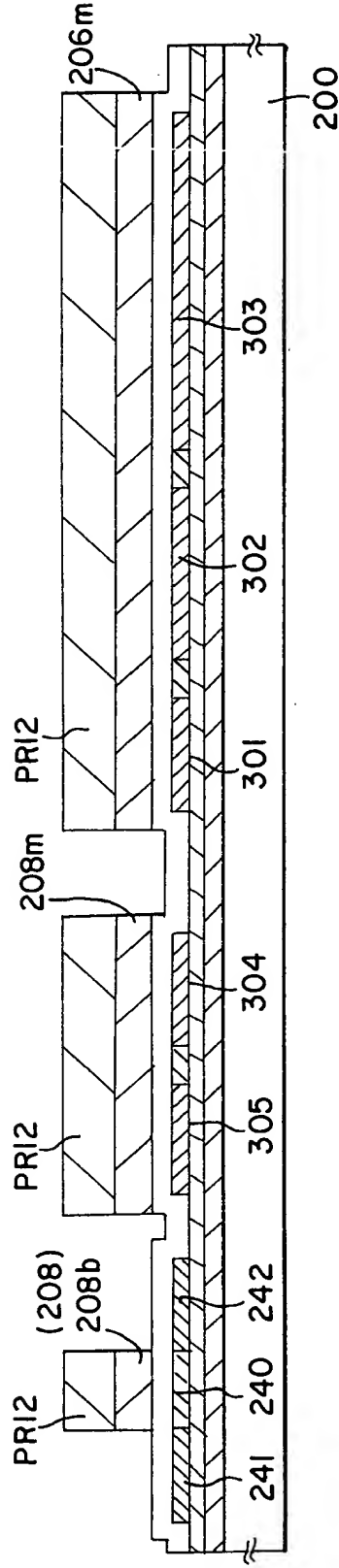
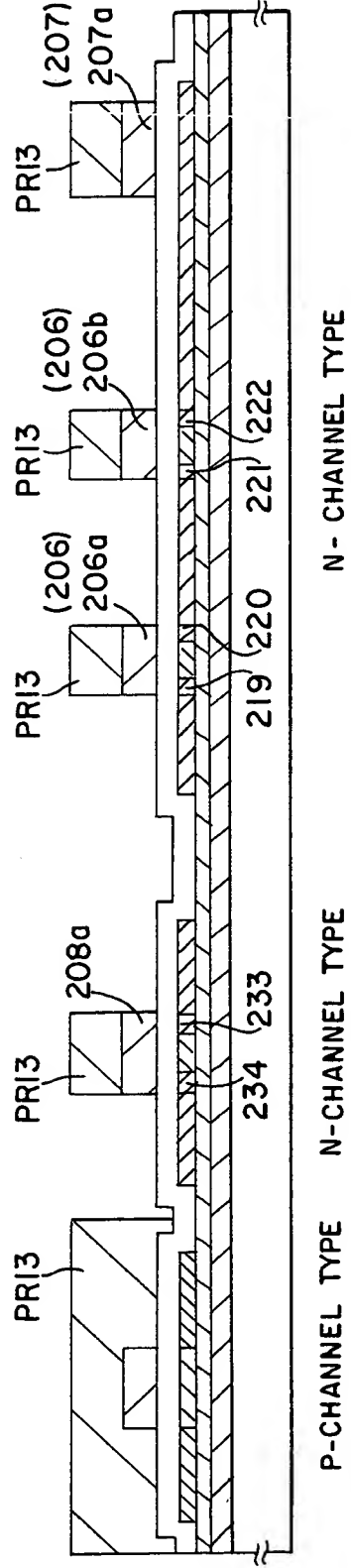


FIG.8(B)

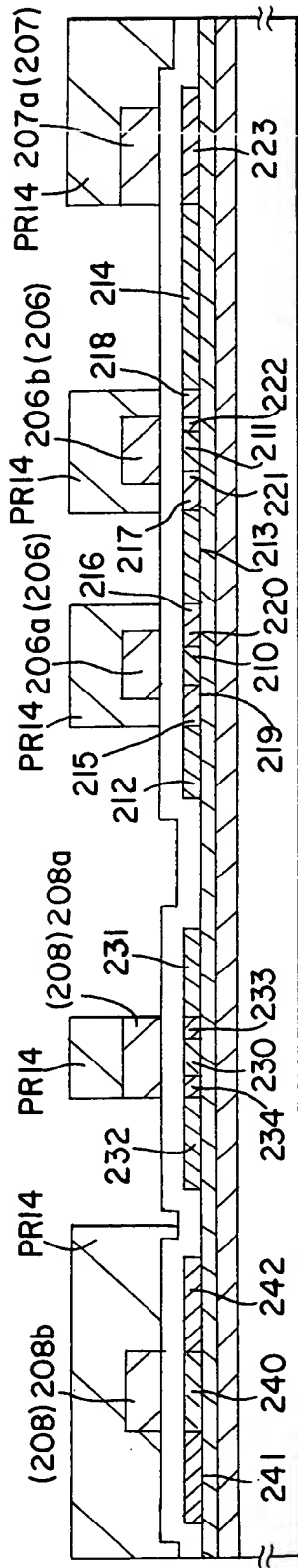
FORMATION OF WIRING





# FIG. 9(A)

DOPING WITH PHOSPHORUS (FORMATION OF  $n^+$ -TYPE REGION)



# FIG. 9(B)

FORMATION OF WIRING AND ELECTRODE

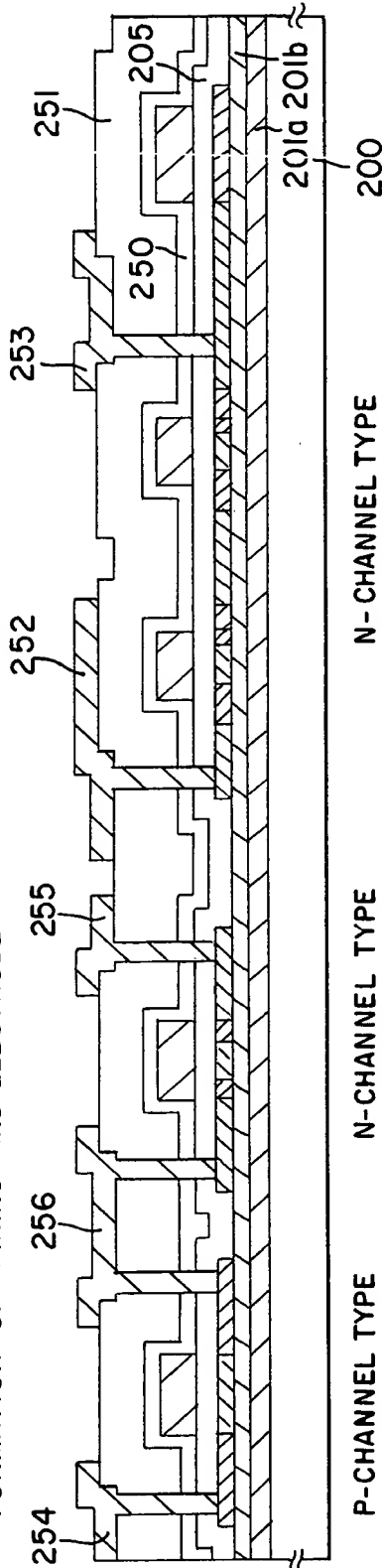
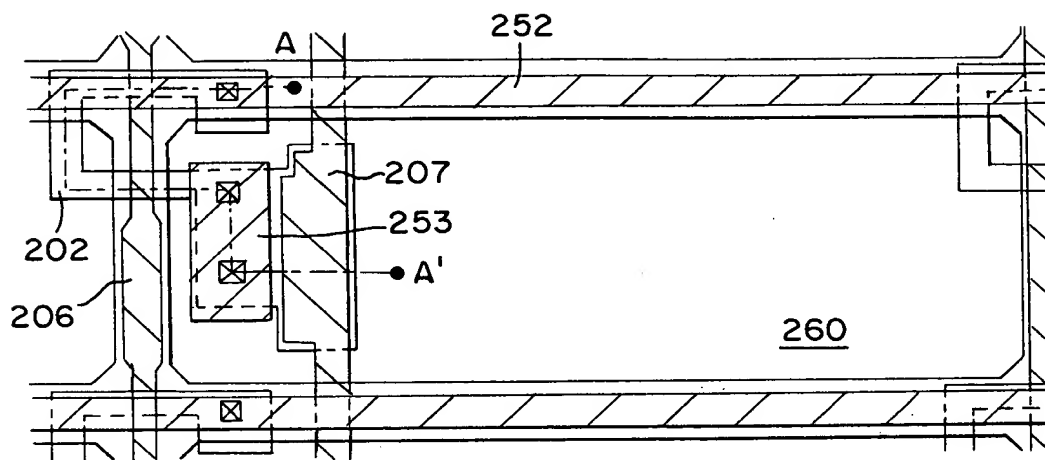


FIG. 10



PLAN VIEW OF PIXEL MATRIX CIRCUIT

FIG. 11

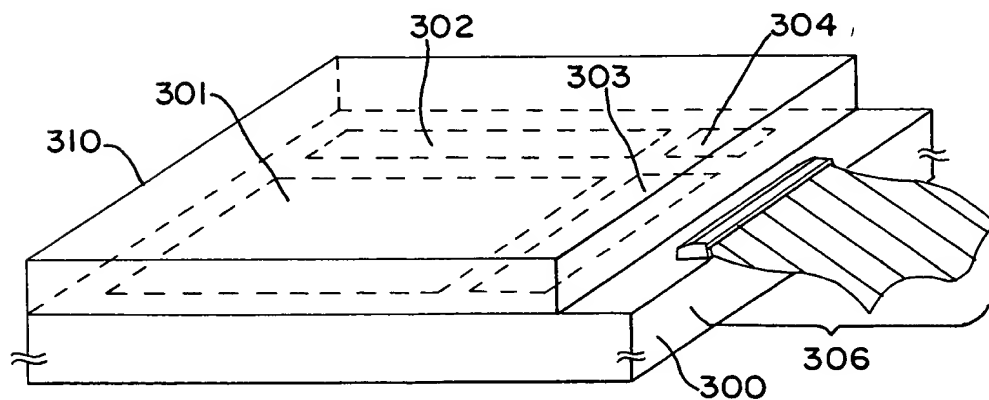


FIG. 12(A)

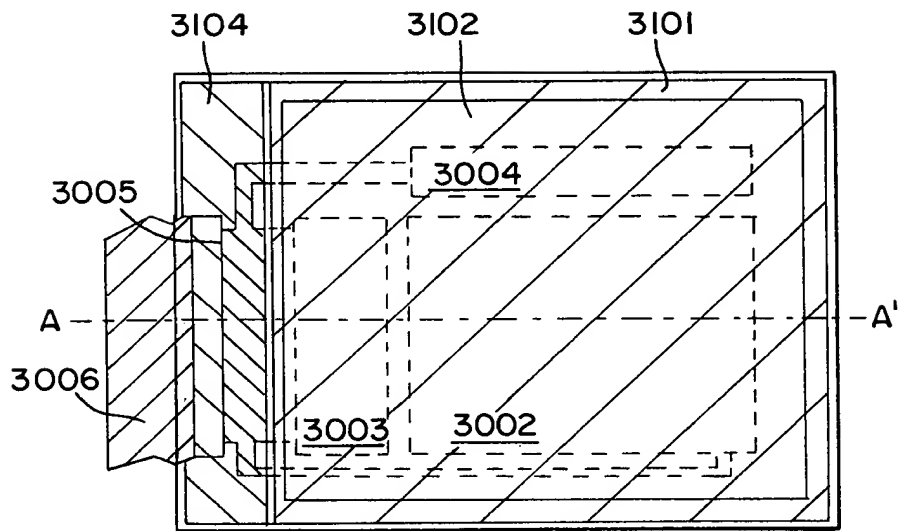


FIG. 12(B)

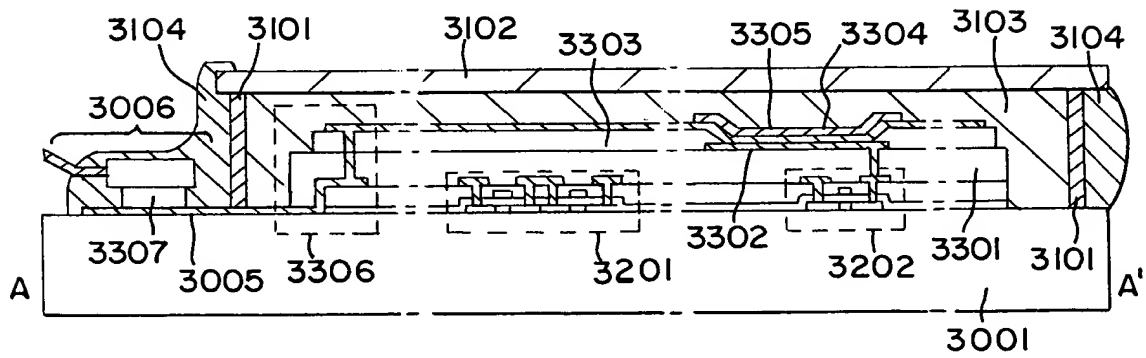


FIG. 13(A)

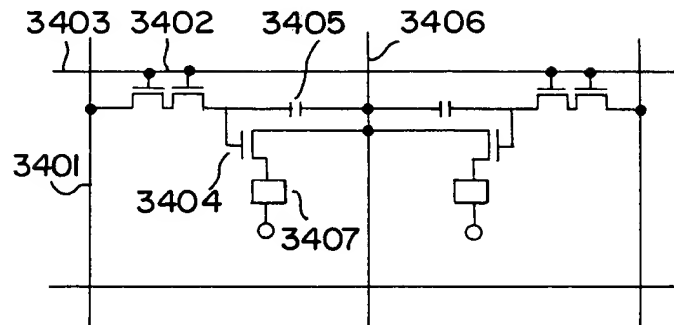


FIG. 13(B)

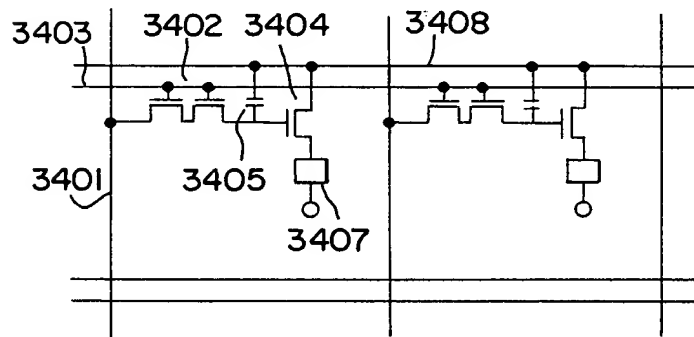


FIG. 13(C)

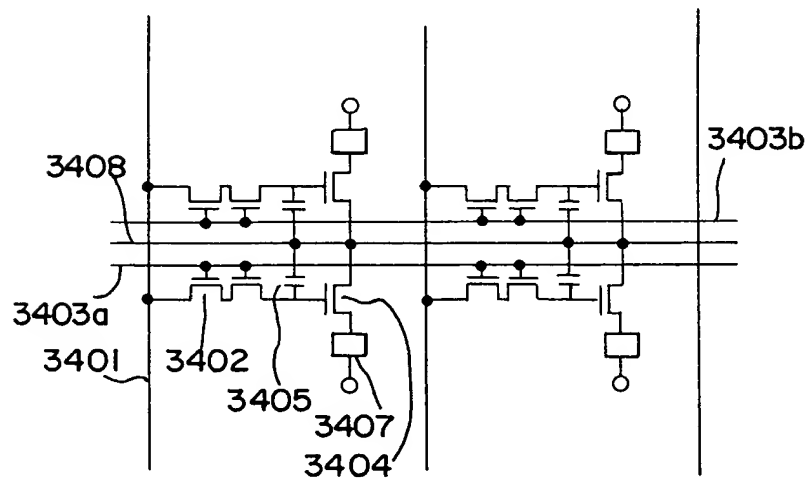


FIG. 14(A)

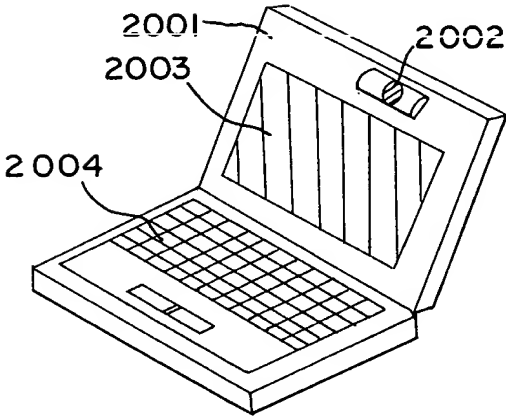


FIG. 14(B)

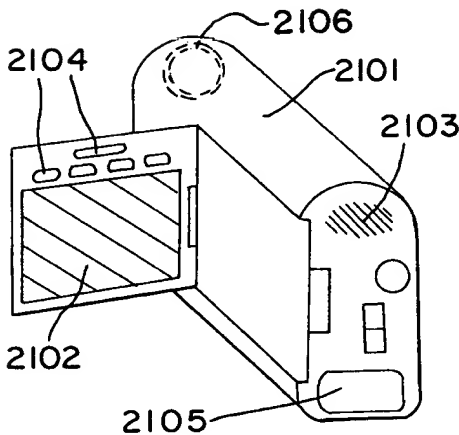


FIG. 14(C)

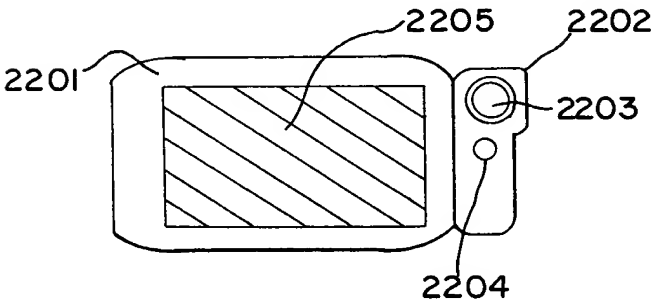


FIG. 14(D)

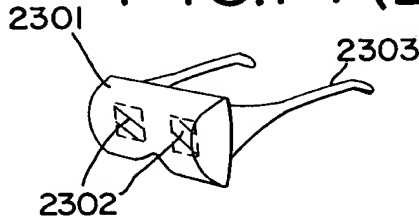


FIG. 14(E)

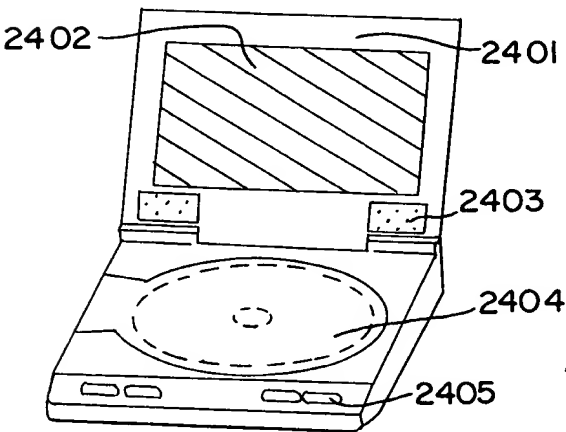


FIG. 14(F)

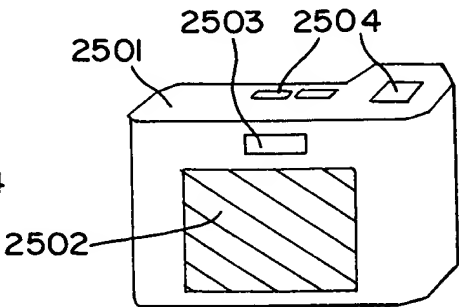


FIG. 15(A)

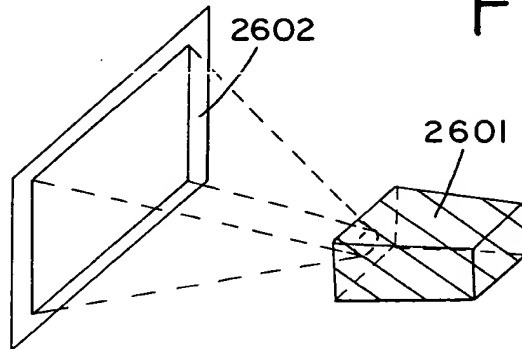


FIG. 15(B)

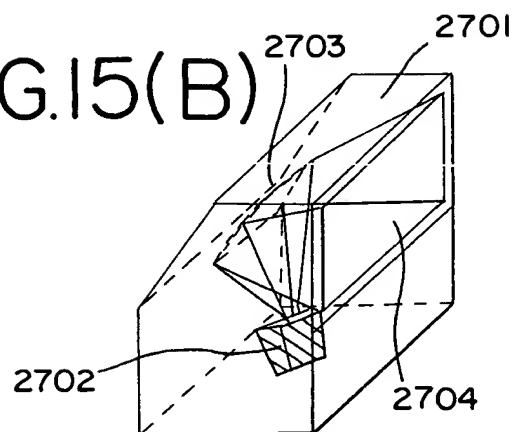


FIG. 15(C) PROJECTION UNIT (THREE-LENS TYPE)

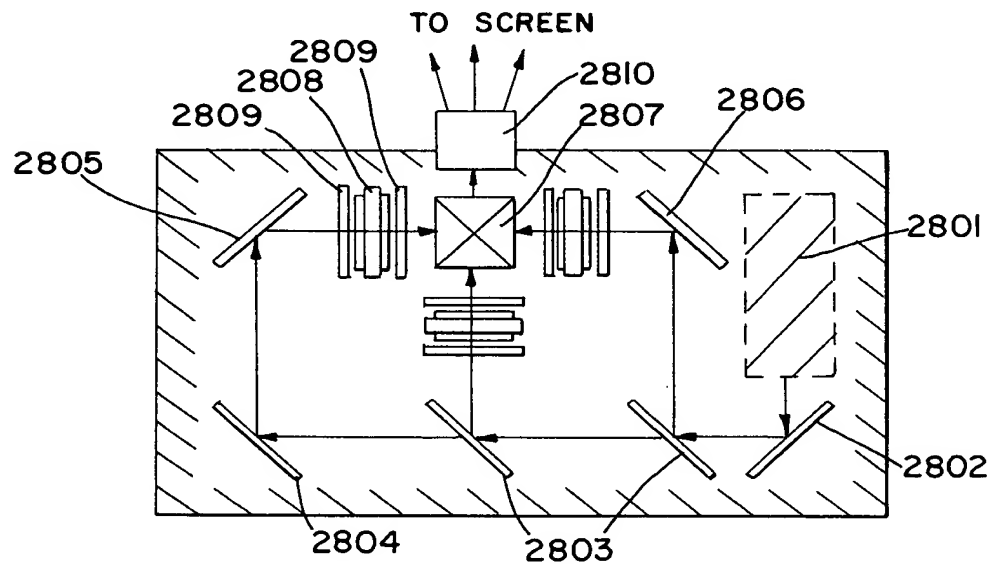


FIG. 15(D)

LIGHT SOURCE  
OPTICAL SYSTEM

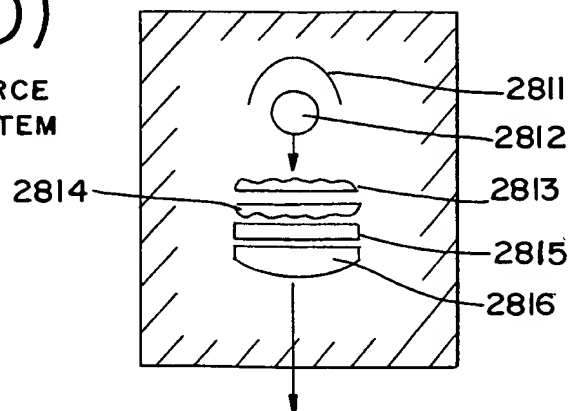


FIG. 16(A)

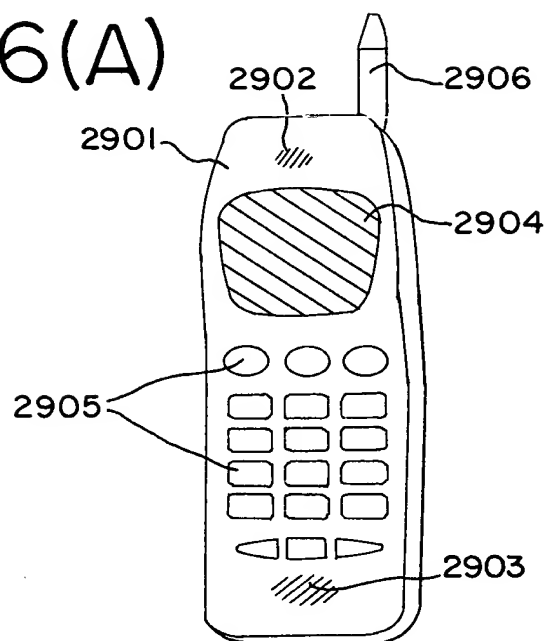


FIG. 16(B)

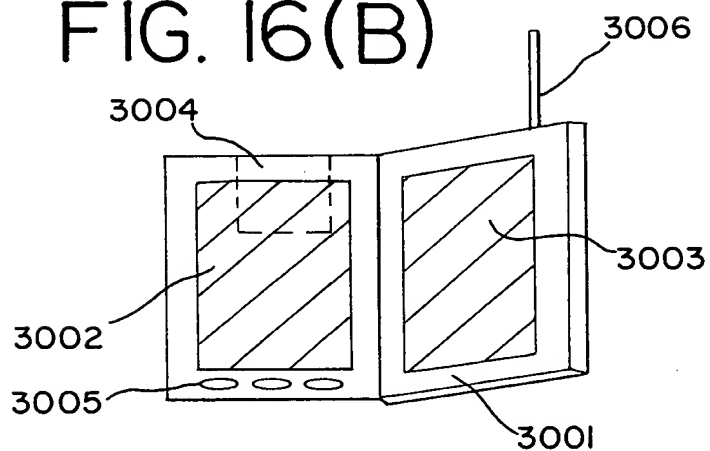


FIG. 16(C)

